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FLETCHER YODER (MICRON TECHNOLOGY, INC.)
P.O. BOX 692289
HOUSTON, TX 77269-2289

EXAMINER	
TOLEDO, FERNANDO L	

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte PAUL SHIRLEY and GORDON HALLER

Appeal 2009-2352
Application 10/765,481
Technology Center 2800

Decided[1]: May 14, 2009

Before KENNETH W. HAIRSTON, JOHN A. JEFFERY, and BRADLEY W. BAUMEISTER, *Administrative Patent Judges*.

BAUMEISTER, *Administrative Patent Judge.*

Opinion Concurring-in-Part and Dissenting-in-Part filed by *Administrative Patent Judge* JEFFERY.

DECISION ON APPEAL

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134 (2002) from the Examiner's final rejection of claims 1-12. We have jurisdiction under 35 U.S.C. § 6(b) (2002). We reverse the rejections of record. We enter new grounds of rejection as to pending claim 12 pursuant to our authority under 37 C.F.R. § 41.50(b).

A. Appellants' invention

Appellants' invention relates to the fabrication of integrated circuits on a semiconductor wafer and, more particularly, to a method of soft baking a semiconductor wafer so that photo resist layers are free of surface voids or craters (App. Br. 2).

B. The claims

Independent claims 1 and 12 are illustrative and read as follows:

> 1. A method of soft-baking a semiconductor wafer substrate, comprising the acts of:
>
> (a) soft-baking a substrate coated with a resist at a first temperature for a first predetermined period of time; and
>
> (b) after act (a), soft-baking the substrate coated with the resist at a second higher temperature for a second predetermined period of time.
>
> 12. A semiconductor wafer comprising a resist layer without craters at the completion of a two-part soft bake of the semiconductor wafer.

C. The reference and rejections

The Examiner relies on the following prior art reference to show unpatentability:

S. WOLF & R. N. TAUBER, SILICON PROCESSING FOR THE VLSI ERA VOLUME 1—PROCESS TECHNOLOGY 429, 434-437, 452 and 453 (Lattice Press 1986) (hereinafter "Wolf").

1. Claims 1-8, 11 and 12 stand rejected under 35 U.S.C. § 102(b) as anticipated by Wolf and Tauber [hereinafter Wolf].
2. Claims 9 and 10 stand rejected under 35 U.S.C. § 103(a) as obvious over Wolf.

Rather than repeat the arguments of the Appellants or the Examiner, we refer to the Brief and the Answer for their respective details.[2] In this decision, we have considered only those arguments actually made by Appellants. Arguments which Appellants could have made but did not make in the Briefs have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

ISSUES

The Examiner asserts that Wolf discloses a two-step process for soft-baking a semiconductor wafer coated with a photoresist, the two-step

[2] We refer to (1) the Appeal Brief filed Nov. 13, 2006; (2) the Examiner's Answer mailed Oct. 31, 2007 and (3) the Reply Brief filed Jan. 4, 2008 throughout this opinion.

process comprising a first, lower-temperature baking step and a second, higher temperature backing step (Ans. 3). More specifically, the Examiner interprets the initial temperature-ramp-up period of Wolf's infrared (IR) oven baking process, which is depicted in figure 20(c), as reading on the first, lower-temperature baking step. The Examiner interprets the steady-state heating portion of the IR oven baking process as reading on the second, higher-temperature baking step (Ans. 7-8). The Examiner states that it is reasonable to interpret the first heating step as reading on the ramp-up period because the "Appellant is [sic: claims are] silent as to [whether] the first temperature is constant for a time period" (Ans. 7).

Appellants assert that the Examiner's interpretation is unreasonably broad and not consistent with the Specification (App. Br. 4-13; Reply Br. 2-4). Citing *Phillips v. AWH Corp*. 415 F.3d 1303 (Fed. Cir. 2005) (en banc), Appellants argue that the Examiner improperly ignores the Specification in interpreting the claim language as required by the Federal Circuit (Reply Br. 3). More specifically, Appellants argue (1) the plain language of claim 1 (in light of the Specification) requires the wafer be subjected to a given, substantially constant, first baking temperature for a period of time; (2) Wolf teaches a typical single-step soft bake—not a two-step soft-bake; and (3) Wolf's ramp-up period for the single-step bake process does not read on the first step of claim 1 because the instantaneous temperature changes occurring during the temperature ramp do not constitute baking at "*a* temperature for a *period* of time" (Reply Br. 2-3; emphasis in original).

The issues before us, then, are:

I. whether Appellants have shown that the Examiner erred in finding that the ramp-up period of Wolf's single-step soft bake process can be reasonably interpreted as constituting "soft-baking a substrate coated with a resist at a first temperature for a first predetermined period of time" as required by claim 1;

II. whether the limited portions of Wolf made of record alone disclose that a semiconductor wafer subjected to a single-step soft-bake process will, at least in some circumstances, produce a resist layer that is free of resist craters, as required by claim 12;

III. whether disclosures within the Specification and Appellants' additional statements on the record can be reasonably interpreted as constituting an admission by Appellants that the single-step soft bake process constitutes prior art; and

IV. whether product claim 12 is nonetheless anticipated by Appellants' prior-art admissions.

FINDINGS OF FACT

The record supports the following Findings of Fact (FF) by a preponderance of the evidence:

1. Wolf expressly states, "[s]everal types of ovens have been developed to implement soft-bake processes… Each employs a different heat transfer mechanisms… Nevertheless they all seek to provide uniform, controlled temperatures and cleanliness" (Wolf, p. 435).

2. Wolf explains that a soft-baking process in convection ovens entails soft-bake cycles of about 30 minutes and requires 6-8 minutes until the wafer temperature approaches oven ambient (Id.).

3. Convection ovens have several limitations including two relating to undesired temperature fluctuations: (1) temperature variations within the oven cavity may lead to non-uniform baking; (2) moving wafers into and out of the oven causes temperature fluctuations, again leading to bake nonuniformities (Wolf, p. 436).

4. Wolf states that soft-baking in IR ovens is advantageous relative to convection ovens because (1) the "soft-bake times are much shorter than convection oven soft-bake times (3-4 min vs. ~30 min);" and (2) IR ovens more rapidly heat the wafers to the desired temperature (Wolf, p. 436).

5. Wolf states that hot-plate soft-baking is advantageous relative to convection ovens because the resist is heated quickly to the desired temperature and the soft-bake cycle can be short—on the order of 30~60 sec/wafer (Wolf, p. 437).

6. Figure 20(c) of Wolf shows temperature ramp-up times of about one minute for IR heating and a few seconds for hot plate heating (Wolf, p. 436).

7. Wolf is silent as to whether wafers produced according a single-step soft-bake process may be specifically free of craters at the completion of the soft bake process.

8. The portions of Wolf made of record do not describe any additional processes—such as the inclusion of interlayer dielectric (ILD) layers—that may enable the production of resist layers that are specifically crater free.

9. Wolf is also silent as to what pitches or packing densities features on the wafer's surface may have.

10. The DESCRIPTION OF THE RELATED ART subsection of Appellants' Specification describes various fabrication processes used to mass produce integrated circuits on semiconductor wafers (Spec. 2-5).

11. The DESCRIPTION OF THE RELATED ART subsection refers to these processes (*see* FF 10) as "commonly known processes" and "among those commonly used" (Spec. 3).

12. These "commonly used processes" (*see* FF 10, 11) include "ion implantation, sputtering, etching, physical vapor deposition (PVD) chemical vapor deposition (CVD) and variations thereof…" (Spec. 3).

13. The DESCRIPTION OF THE RELATED ART subsection explains that prior to the semiconductor wafer being treated by one of these "commonly used processes" (*see* FF 10-12), a photolithography process is used to produce photomasks on the semiconductor wafer (Spec. 3-4).

14. The DESCRIPTION OF THE RELATED ART subsection explains that the photolithography process used in conjunction with the "commonly used processes" (*see* FF 13) entails coating the semiconductor wafer with a light-sensitive photoresist, performing a "[single-step] soft bake" baking process to remove solvent from the resist and/or to harden the resist layer, exposing the resist-coated wafer to ultraviolet light through a photomask to develop the photoresist layer, and subsequently etching selected portions of the photoresist to produce a desired pattern on the surface of the semiconductor wafer (Spec. 3-4).

15. The DESCRIPTION OF THE RELATED ART subsection explains that the single-step soft bake process is problematic in that "[t]ypically, tens, hundreds, or even thousand of microscopic craters may be formed on a single semiconductor wafer" (Spec. 5).

16. The DESCRIPTION OF THE RELATED ART subsection discloses that the root cause of crater formation is the expansion, during the single-step soft bake process, of air bubbles that are trapped between a semiconductor wafer's densely-packed surface elements/structures and over-bridging layer of resist material (Spec. 4-5).

17. The DESCRIPTION OF THE RELATED ART subsection describes further problems relating to various countermeasures that are already used to avoid the formation of air traps: "the excessive use of ILD material and other inefficient approaches are costly and may not reduce or eliminate the formation of resist craters" (Spec. 5).

18. The DESCRIPTION OF THE RELATED ART subsection concludes by stating that "[t]he present invention may be directed to one or more of the problems set forth above" (Spec. 5).

19. The "DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS" section of Appellants' Specification describes an alternative two-step soft bake process that avoids the crater-formation problem associated with the single-step soft bake process (Spec. 6-13).

20. Appellants state in the Appeal Brief that "[t]he present invention relates generally to the fabrication of integrated circuits and, more particularly, to soft-baking a semiconductor wafer so that photo resist layers

are free of surface voids or craters" (App. Br. 2) and that this goal is achieved by a two-step soft-bake (App. Br. 6).

21. In distinguishing their invention's two-step process from Wolf's single-step process, Appellants refer to Wolf's process as "the typical *single-step* soft-bake" (App. Br. 7).

22. Appellants refer to the temperature used in the single-step process as "traditional" (Reply Br. 4).

23. The Specification never uses the specific term "prior art" to describe the single-step soft bake process.

24. The Specification includes the following prior-art disclaimer:

> [The Description Of The Related Art subsection of the BACKGROUND OF THE INVENTION]…is intended to introduce the reader to various aspects of art that may be related to various aspects of the present invention, which are described and/or claimed below. This discussion is believed to be helpful in providing the reader with background information to facilitate a better understanding of the various aspects of the present invention. Accordingly, it should be understood that these statements are to be read in this light, and not as admissions of prior art.

(Spec. 2).

25. Appellants have not affirmatively stated, either in the Specification or anywhere in the record, that any portion of the single-step soft-bake process is their own work.

26. Nothing in the record indicates that the Appellants invented any portion of the single-step soft bake process.

27. The Specification's prior-art disclaimer makes no substantive reference to the single-step soft bake subject matter described in the

DESCRIPTION OF THE RELATED ART subsection or to integrated circuitry fabrication generally.

28. Nothing in the record indicates that a resist-coated semiconductor wafer produced by Appellants' two-step soft-bake process will necessarily be structurally different than one produced by the single-step soft-bake process.

29. The Specification states:

> [c]onsecutive layers of [interlayer dielectric] ILD material and/or relatively large amounts of ILD material may fill gaps in the underlying topology and thus reduce the amount of air that is trapped. Furthermore, consecutive, thick layers of ILD may also act as a more effective barrier that reduces the amount of air reaching the resist layer, and thus reduces the number of craters. However, the excessive use of ILD material and other inefficient approaches are costly and may not reduce or eliminate the formation of resist craters.

(Spec. 5).

30. Figure 1 of the Specification depicts voids or air bubbles 20 and 27 in the densely-packed regions 24 having densely-packed features 14A, 14B, but no air bubbles formed below the resist where the resist is conformally coated over the central section 22 (fig. 1; Spec. 7-8).

31. Claim 12 employs the transition word, "comprising."

32. Claim 12 does not require the presence of any surface features on the wafer.

PRINCIPLES OF LAW

1. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior

art reference." *Verdegaal Bros., Inc. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987).

2. During examination of a patent application, pending claims are given their broadest reasonable construction consistent with the specification. *In re Prater*, 415 F.2d 1393, 1404-05 (CCPA 1969); *In re Am. Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004).

3. "[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, *i.e.,* as of the effective filing date of the patent application." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). It is the use of the words in the context of the written description and customarily by those skilled in the relevant art that accurately reflects both the "ordinary" and the "customary" meaning of the terms in the claims. *Ferguson Beauregard/Logic Controls, Div. of Dover Resources, Inc. v. Mega Systems, LLC,* 350 F.3d 1327, 1338 (Fed. Cir. 2003).

> [The claims] are part of 'a fully integrated written instrument,' … consisting principally of a specification that concludes with the claims. For that reason, claims 'must be read in view of the specification…. [T]he specification 'is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.'

Phillips, 415 F.3d at 1315 (internal citations omitted).

ANALYSIS

I

With respect to all of the Examiner's rejections, we find Appellants' arguments to be persuasive. Our conclusion is based, in large part, on the Wolf reference cited by the Examiner. Wolf provides significant insights into the customary meanings one of ordinary skill in the art would attribute to the claim terms, "a [singular] first temperature" and "a predetermined period of time."

Wolf expressly states, "[s]everal types of ovens have been developed to implement soft-bake processes… Each employs a different heat transfer mechanisms… Nevertheless they all seek to provide *uniform, controlled temperatures* and cleanliness" (FF 1; emphasis added). Wolf explains that a soft-baking process in convection ovens entails soft-bake cycles of about 30 minutes and requires 6 ~ 8 minutes until the wafer temperature approaches oven ambient (FF 2). Convection ovens have several limitations including two relating to undesired temperature fluctuations: (1) temperature variations within the oven cavity may lead to non-uniform baking; (2) moving wafers into and out of the causes oven temperature fluctuations, again leading to bake nonuniformities (FF 3).

Wolf also compares soft-baking in IR ovens and on hot plates to convection ovens. Wolf states that soft-baking in IR ovens is advantageous because (1) "the [IR oven] soft-bake times are much shorter than convection oven soft-bake times (3~4 min vs. ~30 min);" and (2) IR ovens more rapidly heat the wafers to the desired temperature (FF 4). Hot-plate soft-baking is advantageous because the resist is heated quickly to the desired temperature and the soft-bake cycle can be short—on the order of 30~60 sec/wafer (FF

5). Figure 20(c) of Wolf shows temperature ramp-up times of about one minute for IR heating and a few seconds for hot plate heating (FF 6).

To summarize, the steady-state temperature is the only temperature that Wolf envisions maintaining intentionally during the IR soft-bake process. Wolf evidences that one of ordinary skill in the art would understand that a temperature-ramp-up period is undesirable, but unavoidably incidental to all single-step soft-bake processes. Further, the temperature-ramp-up period of an IR process is so short, the sub-period during which any given ramp-up temperature is exhibited would be negligibly small relative to the steady-state IR baking period. As such, one skilled in the art would not reasonably interpret the first, low-temperature baking step of claim 1 as reading on either Wolf's entire ramp-up time or any portion thereof.

The Dissent agrees with the majority's reasoning of why the first, low-temperature soft bake step of claim 1 cannot be reasonably be interpreted as reading on the entire ramp-up period of Wolf's IR baking process (Dissent 31 fn. 11). The Dissent would nonetheless find that Wolf's IR baking process anticipates claim 1 under the alternative theory that the first baking step reads on any one of the specific temperatures that are measured at any particular moment in time within the ramp-up period of Wolf's process (Dissent 31-39). Admittedly, this interpretation is conceivably plausible, but it is not a reasonable interpretation consistent with the Specification.

The Dissent correctly recognizes that monitored heating processes are typically measured with thermometers and controlled with control systems,

both of finite accuracy (Dissent 34-36). We agree that temperature fluctuations and measurement inaccuracies are inherent to every monitored heating process, regardless of whether the heating process is intended to be carried out in a single step of constant temperature in two or more steps of respectively different temperatures (Dissent 34-36). We also do not question the Dissent's conclusion that, depending upon the accuracy of the particular thermometer used, the temperature *displayed by the thermometer* during the ramp-up period of Wolf's IR heating process may be constant for time periods of approximately 0.8 seconds (Dissent 35). But the temperature displayed by the thermometer is merely a representation of the oven's actual temperature. It is not the actual temperature of the oven itself.

Following the Dissent's rationale, whether any monitored heating process is deemed to be a single-step or multi-step process would be solely dependent upon the accuracy of the thermometer, irrespective of how many separate, discrete heating temperatures are intended. For example, if the thermometer is of sufficiently high quality, one able to measure every minor but unavoidable temperature fluctuation, then even every heating process intended to be carried out at a constant temperature would be deemed to be a multi-step heating process. This is so because the highly accurate thermometer would display different temperatures during minor, but unavoidable, temperature fluctuations. In such a case, it would never be possible to carry out a "single-step" heating process.

Hence, the Dissent's alternative interpretation conflicts with how the terminology is used in the present Specification. The Specification plainly discloses that a single-step soft baking was known, but that a two-step

baking process has advantages (*see generally*, Spec. 2-5). By disclosing the existence of a single-step (i.e., single-temperature) baking process, the Specification evidences that the Dissent's interpretation, based upon displayed representations of temperature, is too hyper-technical to be reasonable.

The Dissent also correctly asserts that neither claim 1 nor the Specification provides any express definition or clear limits for how short in duration the claimed "first predetermined period of time" may be (Dissent 38). Granted, persons of ordinary skill in the art might well reasonably disagree as to where, within the present context, the lower limit of "a predetermined time" lies. But that issue is not before us, and we need not resolve it. It suffices to note that whatever the lowest reasonable time limit may be, the Specification reasonably indicates that instantaneous temperature changes are below it. The omissions of express definitions and clear limits from the claims and Specification do not justify applying the broadest conceivable interpretation of the claim limitation in complete disregard for the Specification.

The Dissent also notes that Appellants' arguments regarding the creation of crater-free resist films are not commensurate in scope with the language of claim 1 (Dissent 37-39, citing App. Br. 9; Spec. 8-10). This is because claim 2—not claim 1—recites language relating to the absence of

resist craters.[3] The Dissent finds this fact to be a basis to conclude that the Dissent's interpretation of claim 1 is reasonable (Dissent 38-39).

We do agree with the Dissent that claim differentiation principles lead to the presumption that the scope of claim 1 is intended to be broader than the scope of claim 2 (Dissent 37). But the language of claim 2 does not evidence the specific intent that the first soft baking step of claim 1 should be interpreted broadly enough to also read on instantaneous temperature changes. Rather, claim 1 is merely broader than claim 2 in that claim 1 also reads on a two-step soft bake method where at least some resist craters are formed. Claim 2 simply does not shed any additional light on how to interpret either of the terms of claim 1, "a first temperature" and "a first predetermined period of time."

For the foregoing reasons, Appellants have persuaded us of error in the Examiner's anticipation rejection of representative claim 1. Accordingly, we reverse the Examiner's rejection of claim 1 and dependent claims 2-8 and 11 which fall with claim 1.

We also reverse the Examiner's rejection of claims 9 and 10 under 35 U.S.C. § 103 as obvious over Wolf. The Examiner's reasoning for why it would have been obvious to modify the heating temperatures and duration do not cure the deficiencies that we noted in relation to the rejection of claim 1.

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[3] Claim 2 further recites, "[t]he method, as set forth in claim 1, wherein no resist craters are formed."

II

Regarding independent claim 12, Wolf indicates that the number of air bubbles—and therefore resultant resist craters—produced during a single-step soft-bake process may be *sufficiently limited* so as to at least enable the wafer to function for its intended purpose (*see* Wolf, pp. 434-37). However, Wolf is silent as to whether wafers produced according a traditional, single-step soft-bake process may be specifically *free* of craters at the completion of the soft bake process (FF 7). Further, the portions of Wolf made of record do not describe any additional processes—such as the inclusion of ILD layers—that may enable the production of resist layers that are specifically crater free (FF 8). Wolf is also silent as to what pitches or packing densities features on the wafer's surface may have (FF 9). Absent any such additional evidence, which is not disclosed in the cited portions of Wolf itself, we can not interpret Wolf alone as expressly, implicitly or inherently disclosing that the traditional, single-step soft bake process is capable of producing crater-free resists in at least some circumstances.

For the foregoing reasons, Appellants have persuaded us of error in the Examiner's anticipation rejection of claim 12 over Wolf. Accordingly, we also reverse the Examiner's rejection of claim 12.

III

Appellants' Specification includes a section titled, "BACKGROUND OF THE INVENTION" (Spec. 2). This section, in turn, further includes a subsection titled, "DESCRIPTION OF THE RELATED ART" (Spec. 2-5). For the reasons set forth in section III of this decision, we must determine whether

disclosures within the Specification and Appellants' additional statements on the record can be reasonably interpreted as constituting an admission by Appellants that the single-step soft bake process constitutes prior art.

The DESCRIPTION OF THE RELATED ART subsection describes various fabrication processes used to mass produce integrated circuits on semiconductor wafers (FF 10). This subsection refers to these processes as "commonly known processes" and "among those commonly used" (FF 11). These "commonly used processes" include "ion implantation, sputtering, etching, physical vapor deposition (PVD) chemical vapor deposition (CVD) and variations thereof…" (FF 12). This subsection also explains that prior to the semiconductor wafer being treated by one of these processes, a photolithography process is used to produce photomasks on the semiconductor wafer (FF 13).

The DESCRIPTION OF THE RELATED ART subsection explains that this photolithography process entails coating the semiconductor wafer with a light-sensitive photoresist, performing a "[single-step] soft bake" baking process to remove solvent from the resist and/or to harden the resist layer, exposing the resist-coated wafer to ultraviolet light through a photomask to develop the photoresist layer, and subsequently etching selected portions of the photoresist to produce a desired pattern on the surface of the semiconductor wafer (FF 14). The DESCRIPTION OF THE RELATED ART subsection explains that the single-step soft bake process is problematic in that "*[t]ypically*, tens, hundreds, or even thousand of microscopic craters may be formed on a single semiconductor wafer" (FF 15; emphasis added). This subsection explains that the root cause of crater formation is the

expansion, during the single-step soft bake process, of air bubbles that are trapped between a semiconductor wafer's densely-packed surface elements/structures and over-bridging layer of resist material (FF 16). This subsection also describes further problems relating to various countermeasures that are already used to avoid the formation of air traps: "the excessive use of ILD material and other inefficient approaches are costly and may not reduce or eliminate the formation of resist craters" (FF 17). The DESCRIPTION OF THE RELATED ART subsection concludes by stating that "[t]he present invention may be directed to one or more of the problems set forth above" (FF 18). The subsequent "DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS" section of Appellants' Specification describes an alternative two-step soft bake process that avoids the crater-formation problem associated with the single-step soft bake process (FF 19).

Read as a whole, the Specification indicates that Appellants' invention relates solely to the two-step soft bake process, which solves previously-known problems associated with the single-step process: (1) crater formation in soft-baked resists and (2) the need to employ excessive ILD material or other inefficient approaches that are costly and may not reduce or eliminate the formation of resist craters. Restated, the Specification implies that the single-step soft bake process is not part of the Appellants' invention. Rather, the single-step soft bake process constitutes prior art upon which Appellants' inventive two-step soft bake process improves. *See In re Preda*, 401 F.2d 825, 826 (CCPA 1968) (noting that "in considering the disclosure of a reference, it is proper to take into account not only specific teachings of

the reference but also the inferences which one skilled in the art would reasonably be expected to draw therefrom").

Moreover, Appellants have made additional statements during prosecution that support this interpretation. *See In re Lopresti*, 333 F.2d 932, 934 (CCPA 1964) (holding that statements made in the Appellants' Appeal Brief constituted an admission that the invention of another was prior art). Appellants state in the Appeal Brief that their invention specifically relates to soft-baking a semiconductor wafer so that photo resist layers are free of surface voids or craters and that this goal is achieved by a two-step soft bake (FF 20). In distinguishing their invention's two-step process from Wolf's single-step process, Appellants refer to Wolf's process as "the *typical single-step* soft-bake" (FF 21, emphasis added). Appellants also refer to the temperature used in the single-step process as "traditional" (FF 22).

These facts set forth above strongly imply that the single-step soft bake process constitutes prior art. Weighing against these facts though, Appellants' Specification never uses the specific term "prior art" to describe the single-step soft back process (FF 23). Rather, the Specification using terms like "description of the *related* art" to describe the single-step soft-bake process (Spec. 2). Moreover, the Specification even includes the following prior-art disclaimer:

> [The Description Of The Related Art subsection of the BACKGROUND OF THE INVENTION] … is intended to introduce the reader to various aspects of art that may be related to various aspects of the present invention, which are described and/or claimed below. This discussion is believed to be helpful in providing the reader with background information to

> facilitate a better understanding of the various aspects of the present invention. Accordingly, it should be understood that these statements are to be read in this light, and not as admissions of prior art.

(FF 24).

The Specification's omission of the term "prior art" and inclusion of the prior-art disclaimer may initially appear to indicate that Appellants do not consider the single-step soft bake process to constitute prior art. To place these latter, contraindicative factors into the proper context though, we note that patent-application drafters regularly endeavor to avoid the indiscriminate or imprudent use of the descriptive label, "prior art." *See Riverwood Intern. Corp. v. R.A. Jones & Co., Inc.*, 324 F.3d 1346, 1354 (Fed. Cir. 2003) (citing *In re Fout*, 675 F.2d 297, 300 (CCPA 1982)) for the proposition that "section 102 is not the only source of … prior art. Valid prior art may be created by the admissions of the parties"); *In re Nomiya*, 509 F.2d 566, 571 (CCPA 1975) (holding that an Applicant's labeling of certain figures as "prior art," *ipsissimis verbis*, constituted an admission that the pictured subject matter was prior art relative to Applicant's invention); MPEP § 2129[4] (instructing that "the examiner must determine whether the subject matter identified as 'prior art' is applicant's own work, or the work of another. In the absence of another credible explanation, examiners should treat such subject matter as the work of another").

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[4] MPEP § 2129 ADMISSIONS AS PRIOR ART.

We appreciate the patent-application drafters' concerns in this regard. Nonetheless, we can not subscribe to a simplistic and formalistic bright-line rule where a statement in the Specification or elsewhere on the record is treated as a prior-art admission by an Applicant if, and *only* if, the specific words "prior art" are expressly used verbatim. If we were to adopt such a formalist bright-line rule, patent practitioners would be able to avoid the legal consequences of making a prior-art admission by merely substituting for the term "prior art," euphemisms like "related art," "background art," "conventional art," "typical art," and the like. This formalistic approach would also conflict with the requirements and intent of 37 C.F.R. § 10.18,[5] governing the disclosure duties placed upon parties involved in a patent prosecution. In short, such a bright-line rule would improperly elevate a disclosure's form over its substance.

We instead interpret the substantive content of the Specification and the record as a whole. When a review of the record as a whole reasonably implies that—or at least raises a reasonable question of whether—a particular disclosure or statement constitutes a prior-art admission, an Examiner may use such a disclosure or statement in formulating prior-art rejections of claims under 35 U.S.C. §§ 102 or 103. This is so even if the specific words "prior art" are not expressly used verbatim. In such circumstances though, the Examiner must set forth the underlying facts and

[5] 37 C.F.R. § 10.18 SIGNATURE AND CERTIFICATE FOR CORRESPONDENCE IN THE PATENT AND TRADEMARK OFFICE is indented under PART 10 – REPRESENTATION OF OTHERS BEFORE THE PATENT AND TRADEMARK OFFICE.

reasoning leading to the conclusion that a disclosure or statement constitutes a prior-art admission.

Such prior-art rejections, when supported by sufficient facts and reasoning, establish prima facie evidence of the claims' unpatentability and shift the burden of rebuttal to the Applicant. An Applicant cannot then rebut the rejection by merely arguing that the term "prior-art" was never used verbatim. Similarly, an Applicant's noting of the fact that the Specification includes a prior-art disclaimer, may not alone be sufficient to rebut such a rejection in those situations where an Examiner has previously provided a rationale for why the disclaimer is ineffective or unpersuasive. Of course, an Applicant may still rebut such a prior-art rejection with credible and sufficient evidence that the disclosure or statement upon which the Examiner relies does not constitute a prior-art admission. For example, an Applicant can still affirmatively state that the disclosure in question was Applicants' own work,[6] not publicly disclosed more than a year prior to the application's filing.[7] *See e.g., Lopresti*, 333 F.2d at 934 (noting that a Rule 131 affidavit[8]

[6] *See e.g.,* 35 U.S.C. § 102(a) (2002) (barring the grant of a patent if the invention was known or used *by others* in this country or described in a printed publication anywhere before the invention thereof by the Applicant); 35 U.S.C. § 102(e) (2002) (barring the grant of a patent if the invention was described in particular types of patent applications or patents *by another* before the invention thereof by the Applicant).

[7] *See e.g.,* 35 U.S.C. § 102(b) (2002) (barring the grant of a patent if the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States).

[8] 37 C.F.R. 1.131 AFFIDAVIT OR DECLARATION OF PRIOR INVENTION.

may overcome a rejection based upon 35 U.S.C. § 102(e)); *In re Ehrreich*, 590 F.2d 902, 909-10 (CCPA 1979) (holding that the Appellants' explanation that their use of a Jepson-claim format was solely for the purpose of overcoming a double patenting rejection was sufficient to rebut the presumption that Appellants' use of the Jepson-claim format was an implicit admission that the subject matter contained within the claim's preamble constituted prior art).

This substantive interpretation approach is unquestionably more sound than would be any alternative rule wherein a disclosure's substance is subservient to the disclosure's form. The substantive interpretation approach aids in clarifying the record at the earliest possible stage of prosecution. It leads to more compact prosecution in that it obviates an Examiner's potential need to interrupt prosecution for the purpose of issuing a Rule 105[9] requirement for information. Moreover, the Applicant is typically in a much better position than the Examiner to know whether a disclosure or statement made by the Applicant relates to prior art or whether it alternatively relates to subject matter that the Applicant has invented.

To be clear, we are not today altering the existing disclosure duties for any Applicant, practitioner, or any other party to a patent prosecution

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[9] *See* 37 C.F.R. § 1.105 REQUIREMENTS FOR INFORMATION (authorizing USPTO employees to require individuals identified under 37 C.F.R. 1.56(c), or any assignee, to provide such information as may be reasonably necessary to properly examine a patent application).

covered by Rule 1.56(c).[10] Nor are we creating any new disclosure duties for any party. We are not granting Examiners a license to automatically conclude that every single statement contained within a section of a Specification titled "Prior Art," "Background of the Invention'" or the like, constitutes a prior art admission merely by virtue of the statement's placement in such a section. Moreover, we certainly are not suggesting that the present Appellants or their Representatives have attempted to improperly conceal any fact or make any false statement, either by using the term "related art" or by including the cited disclaimer within their Specification.

Rather, we are merely noting that the use of alternative characterizations like "related art" and prophylactic prior-art disclaimers, such as the one included in the present Specification, are commonplace in patent prosecution. We are further clarifying that these alternative characterizations and prior-art disclaimers must be reviewed on a case-by-case basis, and in light of the record as a whole, to determine which disclosures and statements, if any, actually constitute prior-art admissions.

We now apply the principles outlined above to the present case. Appellants have not affirmatively stated, neither in the Specification nor anywhere in the record, that any portion of the single-step soft bake process is their own work (FF 25). Nothing in the record indicates that the Appellants invented any portion of the single-step process (FF 26), much less that they invented this subject matter less than one year prior to the

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[10] *See* 37 C.F.R. § 1.56(c) DUTY TO DISCLOSE INFORMATION MATERIAL TO PATENTABILITY.

filing of the present application. Furthermore, the Specification's prior-art disclaimer makes no substantive reference to the single-step soft bake subject matter described in the DESCRIPTION OF THE RELATED ART subsection or even to integrated circuitry fabrication generally (FF 27). Rather, the disclaimer is so broad and generic that it could be inserted, without any editing whatsoever, as boilerplate into virtually any patent application's Specification.

Accordingly, we find that the portions of the Specification's disclosure relating to the single-step soft bake process for a resist-coated semiconductor wafer constitute admissions of prior art (*see e.g.,* Spec. 2-5; 7:7- 9:10). The Specification's omission of the term "prior art" and inclusion of the boilerplate prior-art disclaimer do not change our conclusion. In view of the record as a whole, these factors are ineffective in shielding Appellants from having their prior-art admissions treated as such.

IV

We now enter a new ground of rejection pursuant to 37 C.F.R. § 41.50(b) (2007). Specifically, we reject claim 12 under 35 U.S.C. § 102(a) as being anticipated by Appellants' prior art admissions.

Claim 12 is directed to a product—a semiconductor wafer comprising a resist layer without craters. The product-by-process language of claim 12—"further requiring an absence of craters *at the completion of a two-part soft bake process*"—does not change the fact that claim 12 is, ultimately, directed to the structure of the wafer. *See In re Thorpe*, 777 F.2d 695, 697, (Fed. Cir. 1985) (citations omitted) (noting that,

> even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process).

Nothing in the record indicates that a resist-coated semiconductor wafer produced by Appellants' two-step soft-bake process will *necessarily* be structurally different than one produced by a prior-art single-step soft-bake process (FF 28). To the contrary, Appellants actually acknowledge that it is possible to make a crater-free resist layer using a single-step soft-bake process.

First, the Specification explains that the root cause of crater formation is the expansion, during the single-step soft bake process, of air bubbles that are trapped between a semiconductor wafer's densely-packed surface elements/structures and over-bridging layer of resist material (FF 16). The Specification acknowledges that it is possible to prevent air bubbles from creating craters when using the prior-art, single-step soft-bake process (FF 29). By stating that the ILD *may not* eliminate resist craters, the Specification implies that the use of ILDs alternatively may, at least in some cases, eliminate the formation of resist craters. *See In re Preda*, 401 F.2d at 826 (noting that "in considering the disclosure of a reference, it is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw therefrom").

Secondly, the Specification acknowledges that air bubbles do not form in regions where the surface elements/structures are *not* densely packed (FF

30). As such, the Specification implies that a single-step soft-bake process will not produce resist craters at least for those semiconductor wafers having no densely-packed features. Id.

We also note that claim 12 employs the open-ended transition word, "comprising" (FF 31), and therefore reads on a resist-coated semiconductor wafer that also has one or more ILD layers. *See Genentech, Inc. v. Chiron Corp.,* 112 F.3d 495, 501 (Fed. Cir. 1997)(noting that "'[c]omprising' is a term of art used in claim language which means that the named elements are essential, but other elements may be added and still form a construct within the scope of the claim"). Claim 12 also does not require the presence of any surface features on the wafer (FF 32), much less require any particular pitch or packing densities for any surface features that may be present on the wafer's surface.

Accordingly, the Specification at least implicitly discloses that a semiconductor wafer possessing at least those structures required by claim 12 may be manufactured according the prior-art single-step soft-bake process so as to be free of resist craters at the end of the process. *See Preda*, 401 F.2d at 826 (noting that "in considering the disclosure of a reference, it is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw therefrom").

CONCLUSION OF LAW

I. Appellants have shown that the Examiner erred in finding that the ramp-up period of Wolf's single-step soft bake process can be reasonably

interpreted as constituting "soft-baking a substrate coated with a resist at a first temperature for a first predetermined period of time" as required by claim 1.

II. The limited portions of Wolf made of record do not alone disclose that a semiconductor wafer subjected to a single-step soft-bake process will, at least in some circumstances, produce a resist layer that is free of resist craters, as required by claim 12.

III. Disclosures within the Specification and Appellants' additional statements on the record can be reasonably interpreted as constituting an admission by Appellants that the single-step soft bake process constitutes prior art.

IV. Product claim 12 is nonetheless anticipated by Appellants' prior-art admissions.

DECISION

(1) The Examiner's rejections of claims 1-12 are reversed.

(2) We reject claim 12 under 35 U.S.C. § 102(a) as anticipated by Appellants' prior-art admissions.

(3) Since we have entered a new ground of rejection, our decision is not a final agency action.

FINALITY OF DECISION

This decision contains new grounds of rejection pursuant to 37 C.F.R. § 41.50(b) (2007). This regulation provides "[a] new ground of rejection pursuant to this paragraph shall not be considered final for judicial review."

Moreover, 37 C.F.R. § 41.50(b) also provides that Appellants, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new grounds of rejection to avoid termination of the appeal as to the rejected claims:

> (1) *Reopen prosecution*. Submit an appropriate amendment of the claims so rejected or new evidence relating to the claims so rejected, or both, and have the matter reconsidered by the Examiner, in which event the proceeding will be remanded to the Examiner. . . .
>
> (2) *Request rehearing*. Request that the proceeding be reheard under § 41.52 by the Board upon the same record. . . .

If Appellants elect prosecution before the Examiner and this does not result in allowance of the application, abandonment or a second appeal, this case should be returned to the Board of Patent Appeals and Interferences for final action on the affirmed rejection, including any timely request for rehearing thereof.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

<u>REVERSED</u>
<u>37 C.F.R. § 41.50(b)</u>

JEFFERY, Administrative Patent Judge, CONCURRING-IN-PART and DISSENTING-IN-PART:

I join the majority in reversing the Examiner's anticipation rejection of claim 12 and entering a new ground of rejection under 37 C.F.R. § 41.50(b) for that claim. But I respectfully dissent from the majority's reversing the anticipation rejection of independent claim 1 and the obviousness rejection of claims 9 and 10.

The dispute before us turns on one key question: Can any temperature within Wolf's initial temperature ramp-up period in the infrared (IR) soft-bake process (i.e., the first minute of the IR soft-bake process) in Figure 20(c) constitute "a first temperature for a first predetermined period of time"?[11] For if it can, then the claim would be anticipated since such a period would correspond to step (a) of claim 1, and the subsequent period (i.e., the constant temperature following the ramp-up period) would correspond to step (b) of the claim.

[11] This issue statement emphasizes that I am assessing the propriety of the Examiner's rejection with respect to particular temperatures within the ramp-up period—not the ramp-up period itself. To the extent that the Examiner's position is based on the entire ramp-up period as corresponding to "a first temperature," I find such a position problematic. *See* Ans. 7 (referring to "*a* ramp-up temperature" and "*the* ramp-up temperature" that "lasts for about one minute") (emphasis added). Since the ramp-up period comprises plural temperatures that collectively represent a temperature gradient (or ramp-up) during the time period, for Wolf to anticipate, there must be a single temperature within this time period that meets the criteria of step (a) of claim 1.

The majority answers "no" to this question (*see* Maj. Op. 11-13), but I respectfully disagree given the sheer scope and breadth of the claim language and the nature of Wolf's initial soft-baking temperature ramp-up period—a period that, as explained below, comprises a number of discrete temperatures that would occur for predetermined periods of time.

Two key limitations in step (a) of claim 1 give rise to the dispute before us: (1) "*a* first temperature," and (2) "a first predetermined *period* of time" (emphases added). Regarding these limitations, I agree with Appellants that the qualifier "a" refers to a single temperature, and a predetermined *period* of time must be a specified duration and not instantaneous.

These distinctions form the basis for Appellants' argument, for Appellants contend that the temperatures during Wolf's ramp-up period are instantaneous, and the wafer is therefore not baked at *a* temperature for a *period* of time during this period. (Reply Br. 2-3; emphases in original.) Appellants reason that because there are an "infinite number of instantaneous temperatures" during the ramp-up period, there would be no *single* temperature at which the wafer was subjected for a predetermined time period. (App. Br. 8; Reply Br. 2-3.) In other words, Appellants' argument is premised on the notion that each of these "infinite" temperatures within the ramp-up period occurs instantaneously: a fleeting moment that is so infinitesimally small so as to not constitute a time period. *See id.*

While theoretically correct, this line of reasoning, in my view, completely ignores the realities of practical temperature measurement and

control which, by their very nature, would yield a number of different temperatures that would occur for predetermined time periods.

As an initial matter, Wolf expressly indicates that the ramp-up period is part of the IR soft-bake process. For example, Wolf notes that using IR ovens for soft-baking is advantageous over convection ovens since soft-bake times are much shorter (3-4 minutes vs. approximately 30 minutes). (Wolf, at 436; FF 4.) Significantly, this four-minute infrared soft-bake time period would include the initial one-minute ramp-up period in the infrared temperature profile in Figure 20(c) since the overall process spans approximately four minutes. *See* Wolf, Fig. 20(c). Therefore, Wolf contemplates the increasing temperature in the ramp-up period as soft-baking the wafer, at least in part.

The majority apparently recognizes this fact, but nonetheless asserts that the ramp-up period is “undesirable” and “unavoidably incidental” to single-step soft-bake processes. (Maj. Op. 13.) I do not reach the same conclusion based on Wolf’s somewhat limited discussion of the soft-baking process and various types of ovens used for that process. *See generally* Wolf, at 434-37.

Wolf does point out several drawbacks of soft-baking IR ovens, including temperature non-uniformity, but this involves temperature variations resulting from various wafers’ different reflectivities and absorption characteristics. *See* Wolf, at 436. Wolf says nothing about this problem being related to the gradually-increasing temperature of the initial ramp-up period. *See id.*

Wolf also discusses other problems with IR ovens including (1) solvent vapors that can coat the IR lamps and consequently change their output, and (2) convection heating of gases used to exhaust vaporized solvents which can convectively heat resist surfaces and contribute to crust formation. *Id.* But none of this discussion even hints at the initial one-minute temperature ramp-up period as contributing to these problems, or any other problem for that matter. Indeed, the initial ramp-up period may very well be *desirable* in an IR soft-bake oven—I simply cannot tell from Wolf's limited disclosure.

In any event, even assuming, for the sake of argument, that such an initial ramp-up period is "undesirable" as the majority asserts, it is nonetheless a part of the soft-bake process as a whole as indicated previously. As such, any temperatures within this ramp-up period that occur for a predetermined time period fully meet limitation (a) of claim 1.

As the Examiner indicates (Ans. 7), Wolf's ramp-up period for the infrared soft-bake process begins at approximately 25°C and reaches 100°C in about one minute. *See* Wolf, Fig. 20(c). As that figure indicates, this temperature increase is approximately linear over this interval. *See id.* Assuming this linearity, the rate of temperature increase during the ramp-up period is approximately 1.25°C per second or an increase of about 1°C every 0.8 seconds.[12]

[12] These values were calculated by dividing the difference in starting and ending temperatures by the time period in seconds as follows: (100°C − 25°C)/60 sec. = 1.25°C per second.

Depending on the resolution and accuracy of the temperature detector used in Wolf's IR soft-baking process,[13] the rate of increase in the ramp-up period would be measured (and perhaps indicated) at a particular interval of time. For example, if the temperature detector's resolution and accuracy limited detecting temperatures in increments of 1°C, it would update its measurement every 0.8 seconds during temperature ramp-up. *See* Wolf, Fig. 20(c). In this example, the wafer would therefore be soft-baked at a single temperature (within a predetermined tolerance of 1°C) for a predetermined period of time dictated by this tolerance ("the temperature measurement time period") which, in this example, is 0.8 seconds.[14]

To be sure, the temperature measurement time period (0.8 seconds in the above example) is quite short compared to Wolf's two-minute time period in which the temperature is substantially constant in the IR soft-

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[13] Although Wolf does not expressly disclose a temperature detector, it is nonetheless implicit given the temperature profiles for various soft-baking methods in Figure 20(c). Achieving this functionality via a temperature detector and control system is likewise implicit to Wolf's disclosure and therefore does not negate anticipation. *See In re Graves*, 69 F.3d 1147, 1152 (Fed. Cir. 1995) ("A reference anticipates a claim if it discloses the claimed invention such that a skilled artisan could take its teachings in combination with his own knowledge of the particular art and be in possession of the invention.") (internal citations, quotation marks, and emphasis omitted).

[14] There are many other examples of such temperature measurement and control in which not only is the detected temperature dictated by the detector's resolution and accuracy, but also the time period in which the temperature is detected. For example, if the detector detected temperatures in increments of 5°C, it would update its measurement every four seconds in Wolf's initial IR ramp-up period. *See* Wolf, Fig. 20(c).

baking process (i.e., from 1-3 minutes). *See id.* But it is a time period nonetheless—a time period in which one temperature (within a given tolerance) would be subjected to the wafer and detected for measurement and control.[15] As such, this time period fully meets the first predetermined time period in claim 1.

This same temperature measurement and control tolerance would also manifest itself in Wolf's steady-state interval (i.e., from 1-3 minutes) as well, for no temperature is perfectly constant without at least some variation. Indeed, it is this inevitable variation in detected temperature that conventionally forms the basis for a feedback signal to automatically control a heater to maintain a substantially constant temperature. And like the initial ramp-up interval, these temperatures, too, would be subject to the inherent measurement and control tolerances noted above.[16]

In reaching this conclusion, I realize that the claimed invention uses a two-stage soft-bake process with an initial lower-temperature step to avoid forming resist craters, and that this improves over single-step soft-bake

[15] Notably, dependent claim 6 recites no lower bound on the first predetermined time period, but merely recites that it is "less than 90 seconds." This claim therefore covers any time period—however short—up to 90 seconds. As such, independent claim 1 (from which claim 6 depends) would likewise not be subjected to such a lower bound either.

[16] It is perhaps for this reason that Appellants utilized the qualifier "substantially" in connection with the constant temperature that the wafer is subjected to during the first step. *See* Reply Br. 3 ("[T]he wafer is subjected to a given temperature for a period of time, and thus *substantially* a constant temperature for a period of time during the first step.") (emphasis added).

processes as Appellants indicate.[17] Appellants' arguments, however, are not commensurate with the scope of claim 1 which does not require avoiding such crater formation. Rather, this result is recited in claim 2—not claim 1. As such, claim differentiation principles alone suggest that Appellants did not envision avoiding the formation of craters in the process of claim 1; otherwise, claim 2 would be superfluous.[18]

Of course, claims are not to be read in a vacuum, but must be given their broadest reasonable interpretation in light of the Specification as it would be interpreted by skilled artisans. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1316 (Fed. Cir. 2005) (en banc) (citations omitted). But such an interpretation must not import limitations from the Specification into the claims. "[A]lthough the specification often describes very specific embodiments of the invention, we have repeatedly warned against confining the claims to those embodiments. . . . [C]laims may embrace different

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[17] *See* App. Br. 9 ("[T]he specification clearly explains that a two-step soft bake is employed in lieu of the traditional single-step soft bake *to avoid the formation of resist craters*."); *see also id.* ("[A] period of time is required for the first step *so that no resist craters are formed* in the subsequent second step at the higher temperature bake.") (emphases added). *See generally* Spec. 8-10.

[18] "The doctrine of claim differentiation creates a presumption that each claim in a patent has a different scope. . . . The difference in meaning and scope between claims is presumed to be significant to the extent that the absence of such difference in meaning and scope would make a claim superfluous." *Free Motion Fitness, Inc. v. Cybex Int'l, Inc.*, 423 F.3d 1343, 1351 (Fed. Cir. 2005) (internal quotation marks and citations omitted).

subject matter than is illustrated in the specific embodiments in the specification." *Id.* at 1323 (citations and internal quotation marks omitted).

In this case, the Specification, at best, merely provides examples of durations for the first time period, but never actually defines its limits, let alone its lower limit. *See, e.g.*, Spec. 10:18-19 (noting that the low bake temperature is "*typically* in the range of 30-90 seconds") (emphasis added). Notably, the Specification indicates that the low-bake time in one embodiment may "be decreased, for example, to 30 seconds *or lower*, depending on various conditions." (Spec. 11:13-15; emphasis added.) The Specification is silent, however, as to how short this time can be.

Nor do the claims clarify this uncertainty. Leaving aside the fact that, unlike claim 2, the process of claim 1 does not recite preventing resist crater formation—the point of novelty of the present invention[19]—the claims all but suggest that there is no clear lower limit to the recited time periods. *See, e.g.,* claim 6 (calling for the first predetermined time period to be "less than 90 seconds" but reciting no lower bound); *see also* claim 10 (same regarding the second predetermined time period).

In short, neither the claims nor the Specification provide any clear limits on the duration of the first time period apart from open-ended ranges and examples from preferred embodiments. As such, I find that the scope and breadth of claim 1 when interpreted in light of the Specification does not preclude the discrete temperatures within Wolf's initial temperature ramp-up period in the IR soft-bake process. These temperatures, in my view, fully

[19] *See, e.g.,* Spec 2:8-10; *see also* App. Br. 2, 9.

meet "a first temperature for a first predetermined period of time" given the scope and breadth of the limitation.

While the temperatures in the ramp-up period may theoretically be infinite as Appellants contend (App. Br. 8; Reply Br. 2-3), they are not as a practical matter. Rather, these temperatures are detected and used by instrumentation with real-world limits and tolerances which, by their very nature, would yield a number of different temperatures that would occur for predetermined time periods as explained above.

I therefore respectfully dissent from the majority's reversal of the Examiner's anticipation rejection of independent claim 1. I also respectfully dissent from the majority's reversal of the obviousness rejection of claims 9 and 10 since Appellants' arguments (App. Br. 12-13; Reply Br. 5-6), in my view, do not persuasively rebut the Examiner's prima facie case of obviousness based on Wolf for the reasons indicated above and in the Answer (Ans. 5-7).

gvw

FLETCHER YODER (MICRON TECHNOLOGY, INC.)
P. O. BOX 692289
HOUSTON, TX 77269-2289